

# ESD Protection for Automotive Ethernet Applications

A. Hardock, L. Droemer



Ethernet & IP @ Automotive Technology Week

3<sup>rd</sup>/4<sup>th</sup> November 2021

# Agenda

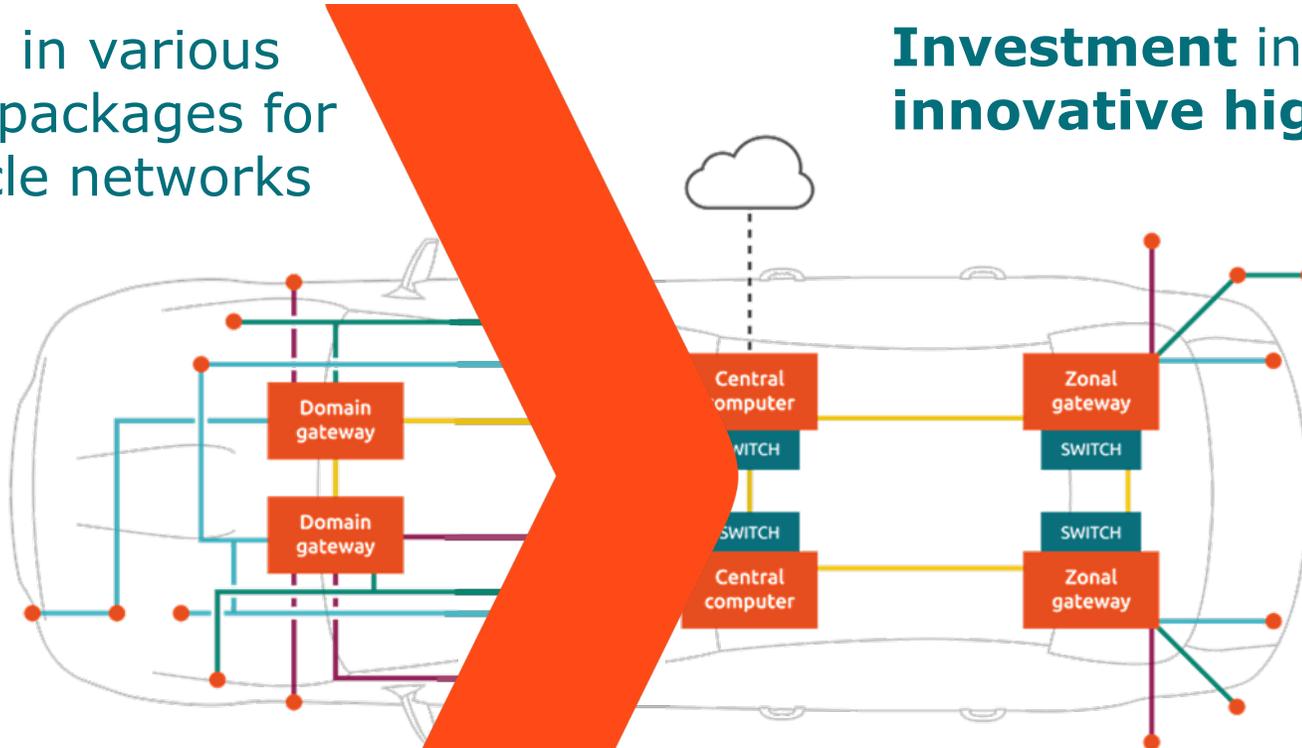
- Introduction to ESD
- SEED Simulation for robust system design
- Multigigabit Ethernet
- Conclusion and Outlook

# Automotive mega trends shaping IVNs

ESD protection fulfilling ISO norms exceeding AEC-Q101 qualification

ESD protection in various footprints and packages for classic in-vehicle networks

- LIN
- CAN
- FlexRay
- SENT
- USB2.0
- HDMI



Investment in R&D with focus on innovative high-speed solutions

- LIN
- CAN-FD/XL
- 10BASE-T1S
- 100BASE-T1
- 1000BASE-T1
- MGBASE-T1
- SerDes
- USBx
- HDMIx
- ILaS
- 5G



From classic **flat wiring harness** to ...

... modern domain and **future zonal architecture**

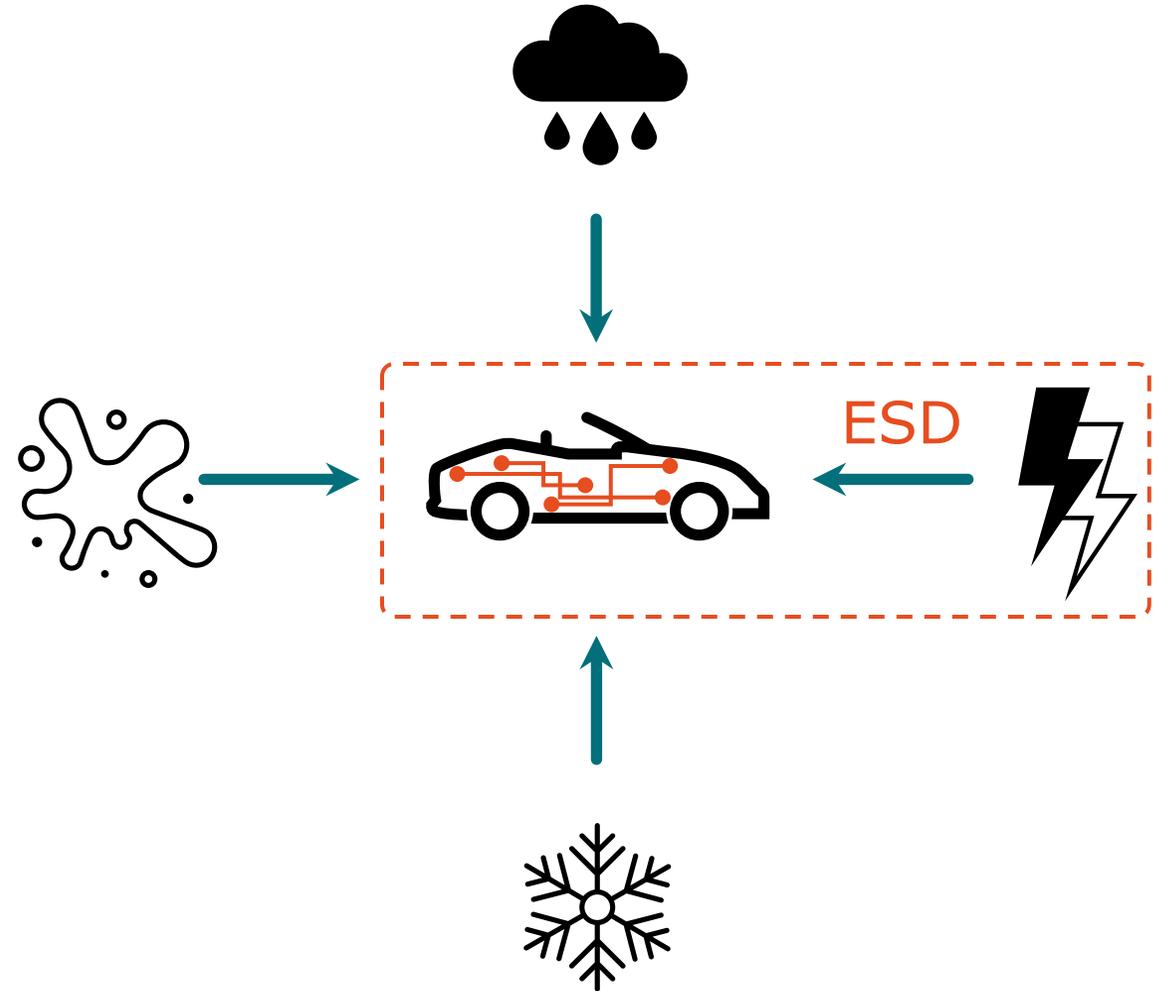
# Automotive Compliance Testing

## Environmental Testing

- Life Profile
- Mechanical
- Climate
- Chemical
- ...

## Electrical Testing

- Functional
- Board net Pulses
- EMC
- **ESD (e.g. IEC61000-4-2)**
- ...



# ESD – Electro Static Discharge

## WHAT

A sudden discharge between persons, devices or components

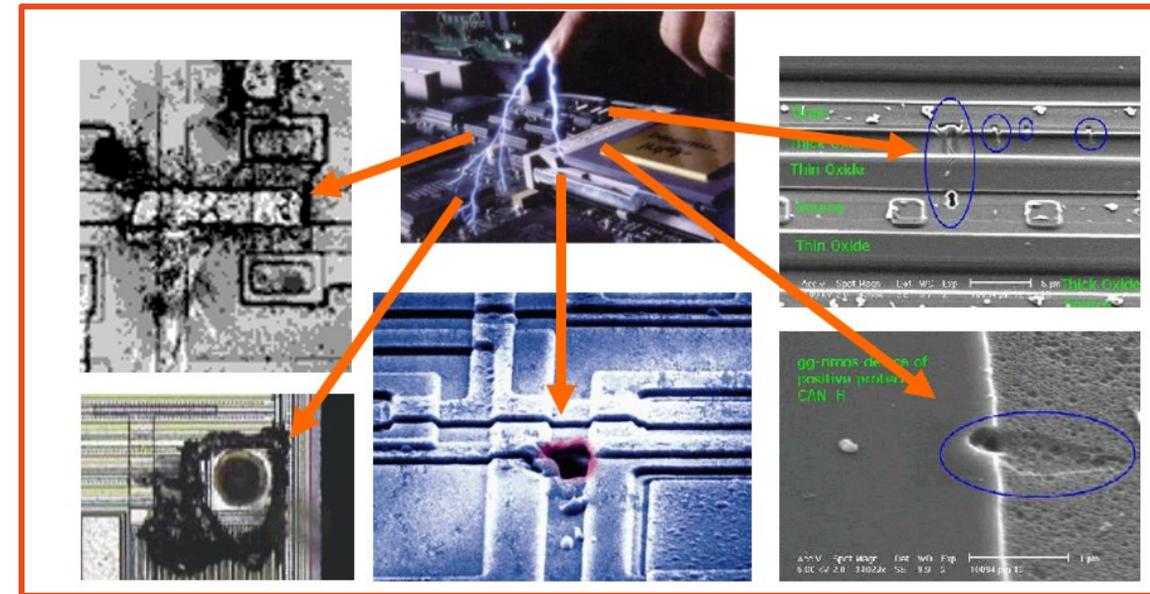


## HOW

- A charged person touches an integrated circuit (IC)
- An electrostatic field is induced by high voltages
- A charged IC drops on a grounded metal plate
- A charged machine touches an IC

## PROBLEM

- Causing malfunction (reversible by power-off-on cycle)
- Destruction of electrical components (irreversible): gate oxide, metallisation or PN junctions



# New IC requirements shape ESD threat

## MEGA TRENDS



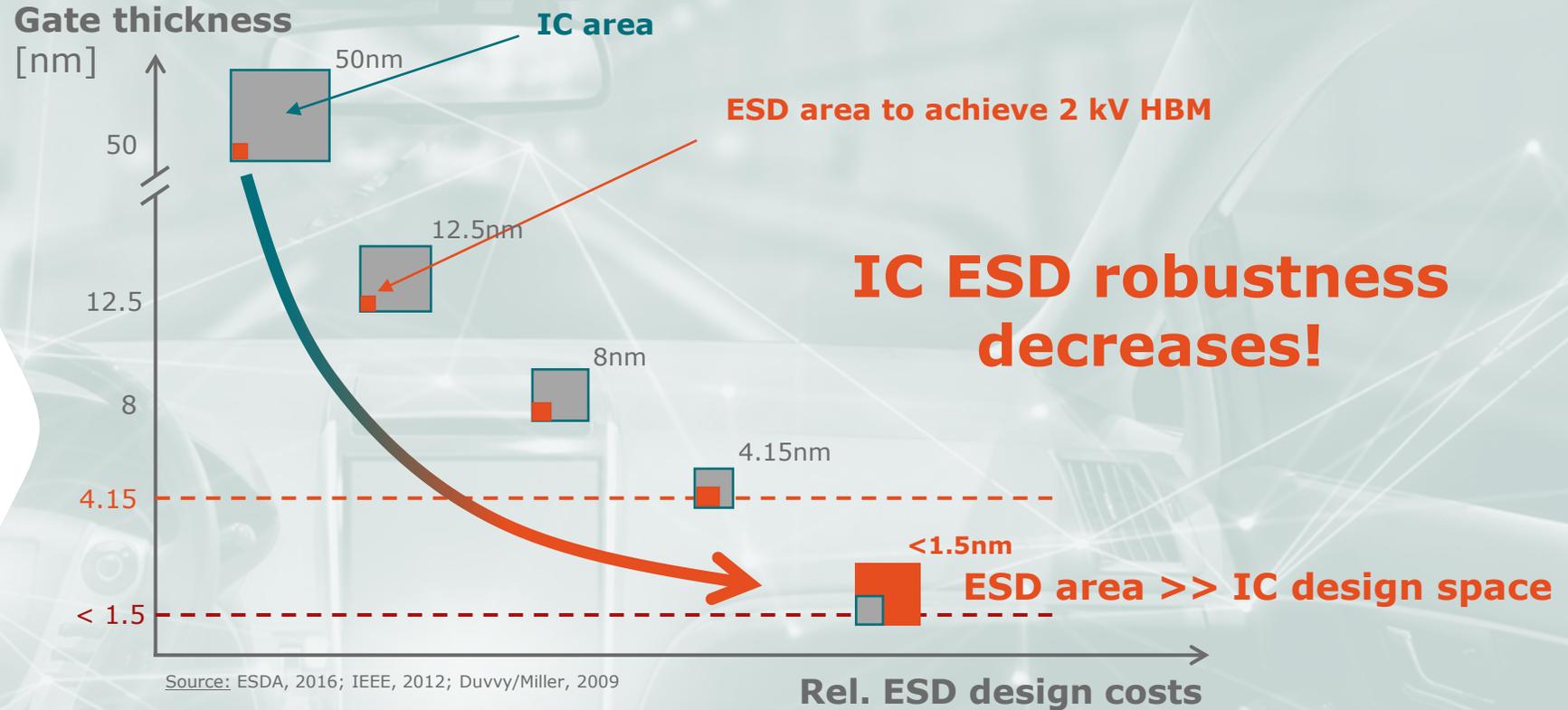
Connected & Autonomous



Electrified

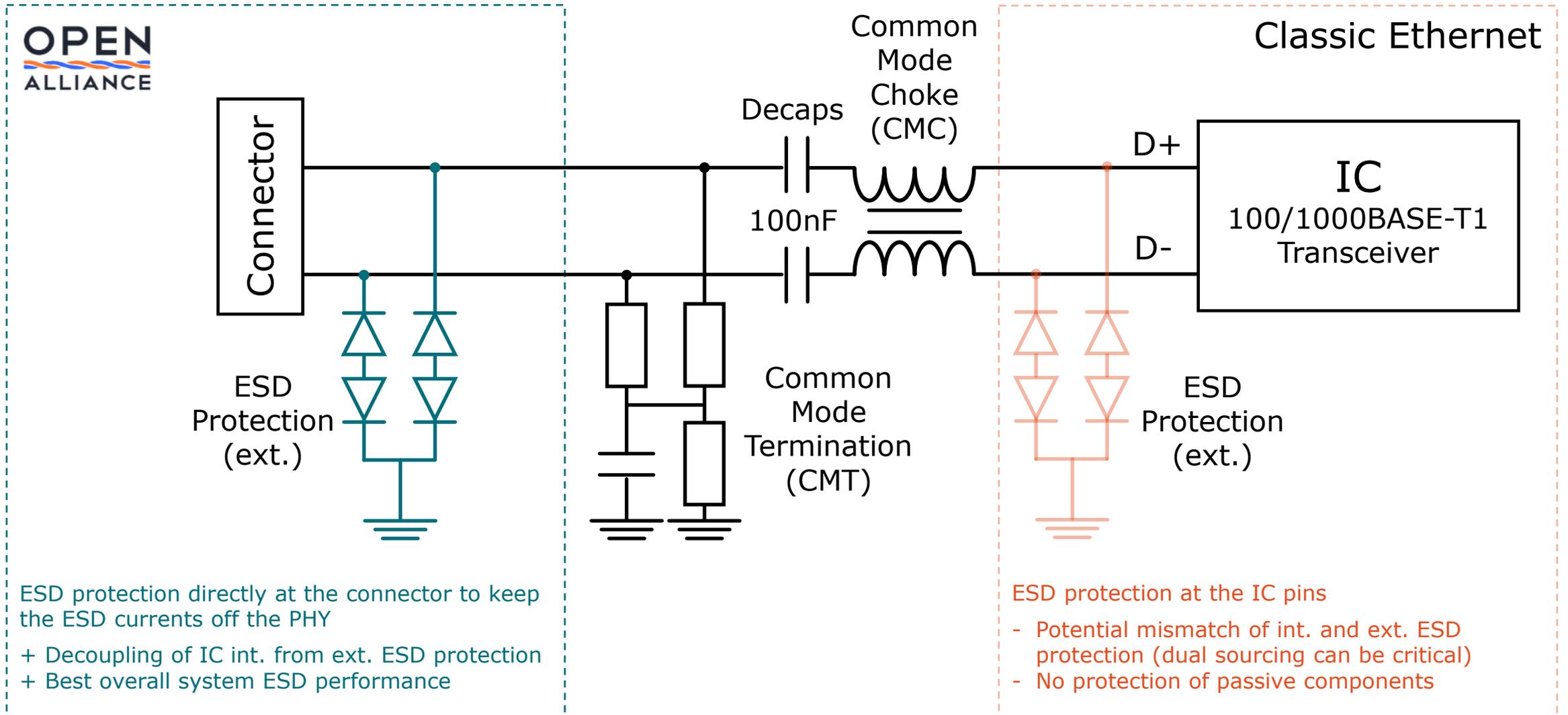


Shared Mobility



**That requires dedicated system-level ESD solutions!**

# OPEN Alliance vs. Classic Ethernet



# OPEN Alliance Spec. for ESD protection devices

## General requirements

### General requirements for 100/1000BASE-T1

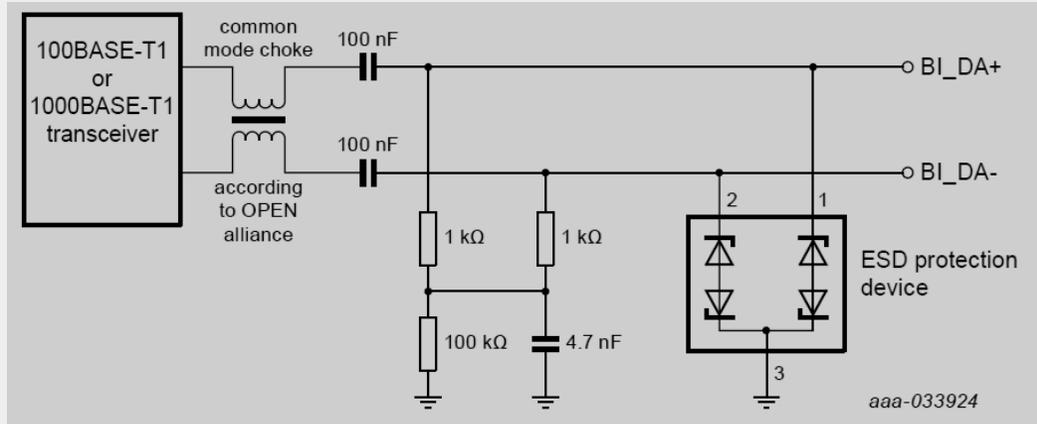
- Trigger voltage  $> 100V$ ,  $V_{DC,max} > 24V$
- Bi-direction device, 15kV IEC, 1000 discharges

### ESD discharge current measurement

- Quantification of the current that would flow into the PHY

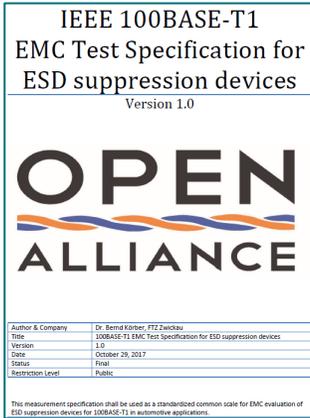
### Additional tests:

- Mixed mode S-parameter measurements
  - To evaluate transmission, symmetry, and mode conversion, replaces requirements on  $C_p$  and matching
- Damage from ESD
  - To verify degradation, first measure S-parameters, apply ESD (8kV) discharges, and check S-parameters again
- Unwanted clamping
  - Evaluate impact of ESD device onto RF immunity testing



# Proof of Concept via measurements

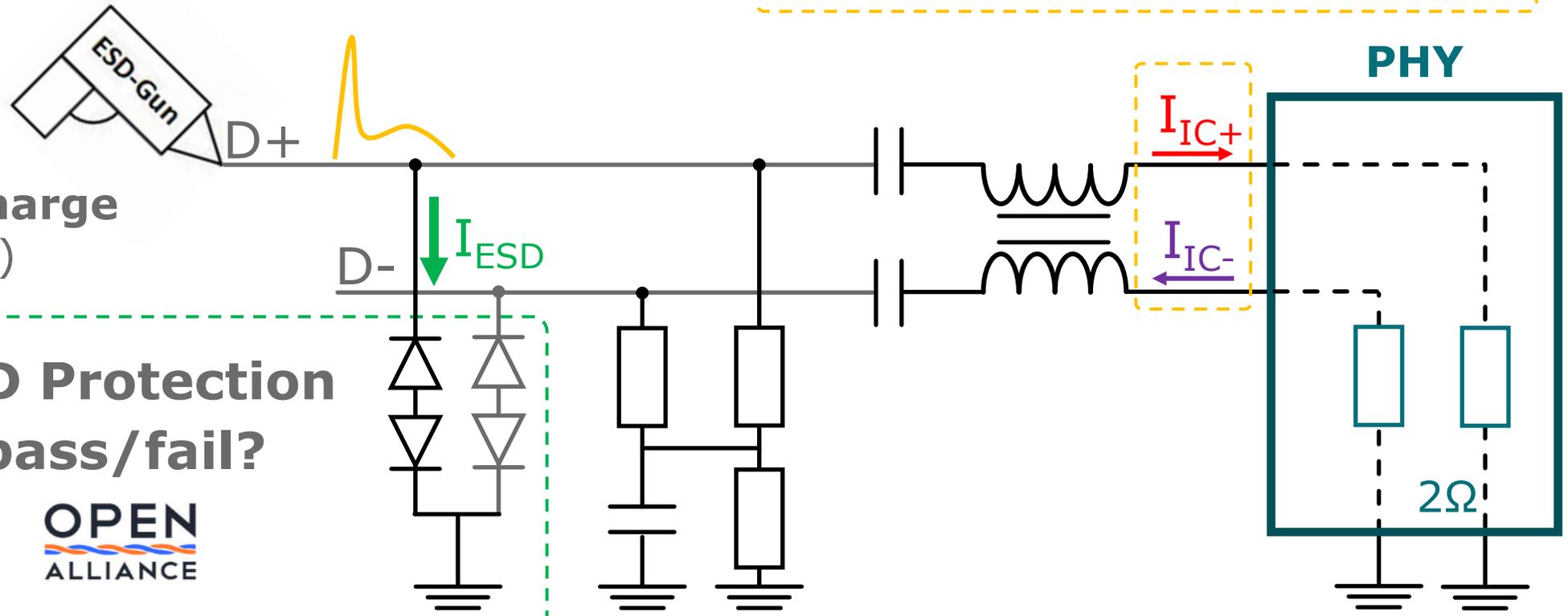
Determines the residual current flowing into IC (PHY) during an ESD event



**ESD Gun Test on PCB**  
(acc. IEC61000-4-2)

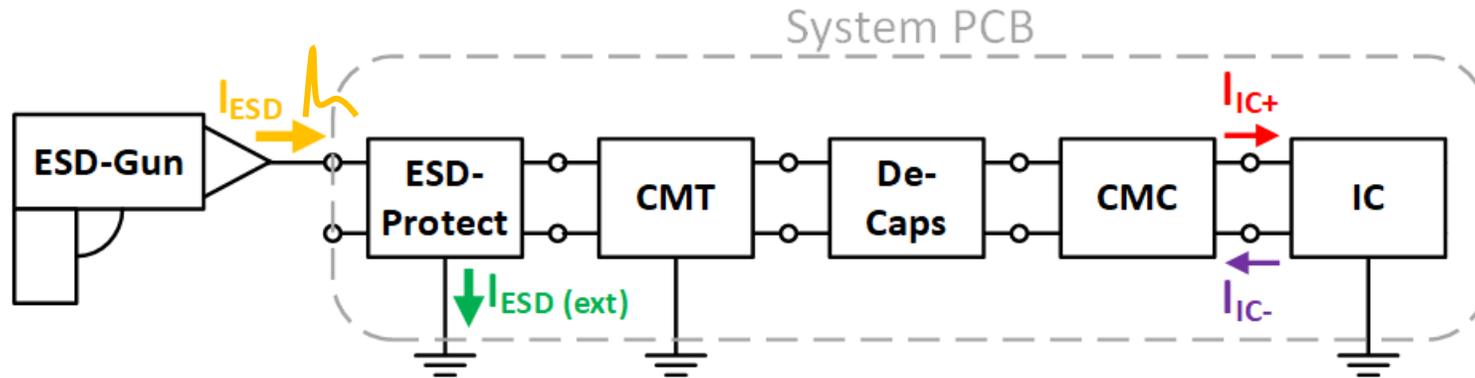
**Evaluation of  
IC current limits acc. HBM**

**Contact discharge**  
4kV (6kV)



# Idea of System Efficient ESD Design (SEED)

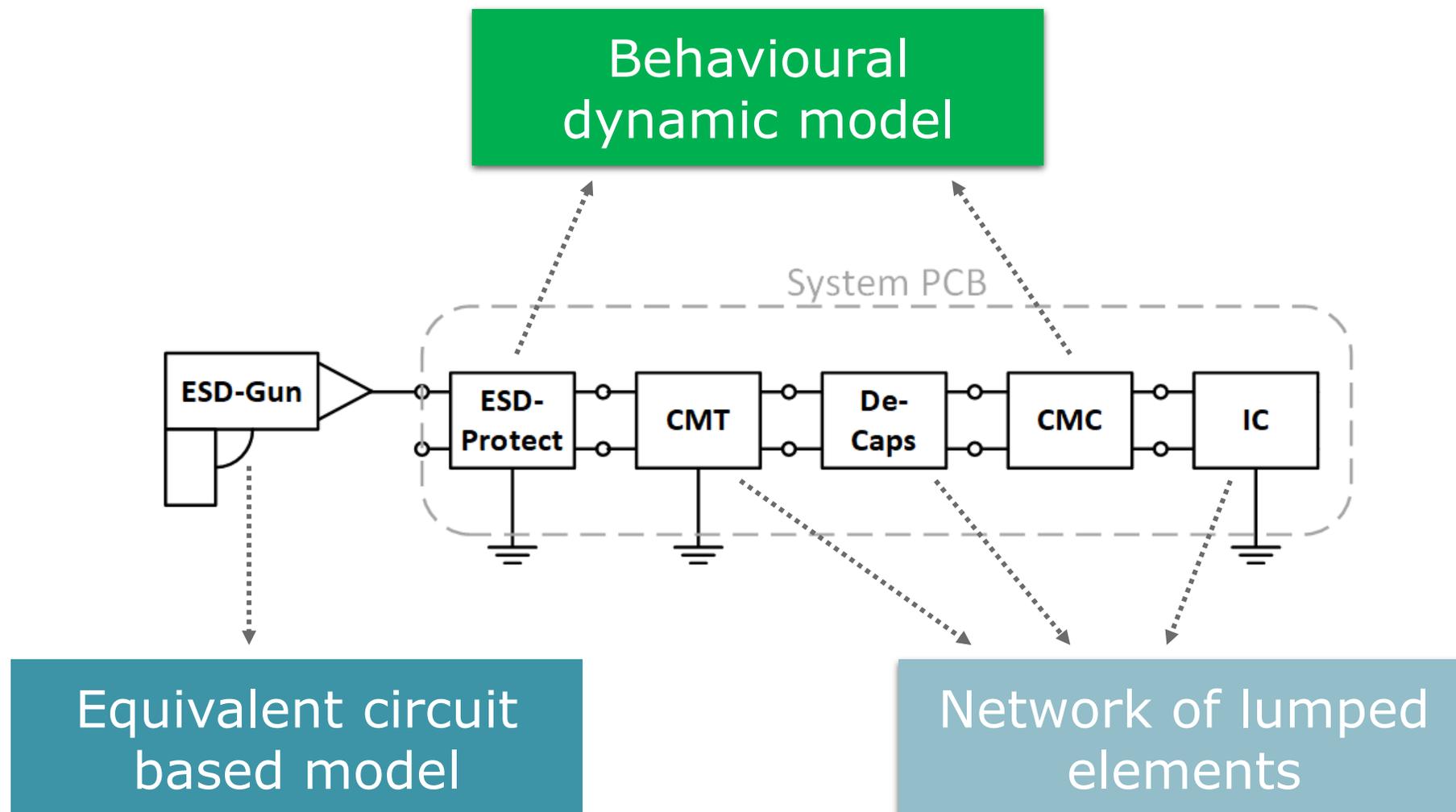
System modelling for transient system-level ESD analysis via simulation



- Evaluation of currents into IC during ESD event
- Prediction of System-level ESD Robustness
- System improvement using Virtual Prototyping
- Reduction of engineering loops (time & cost)

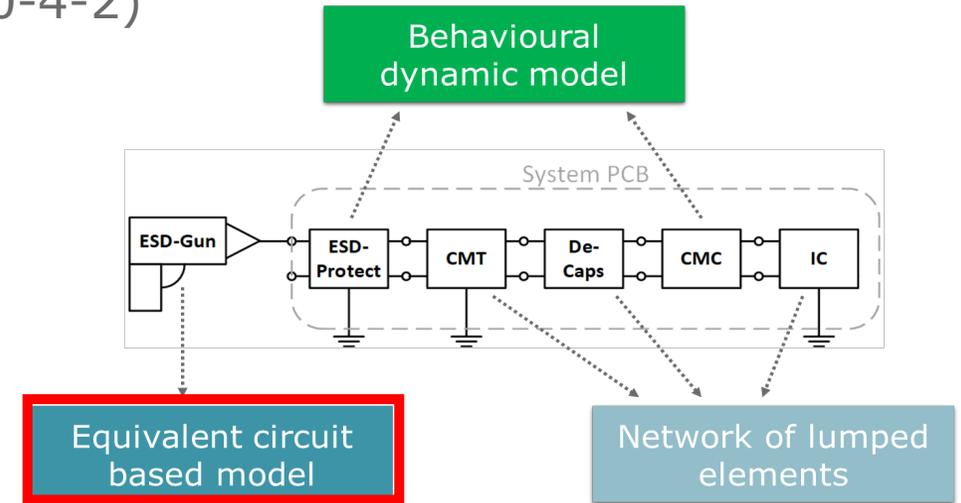
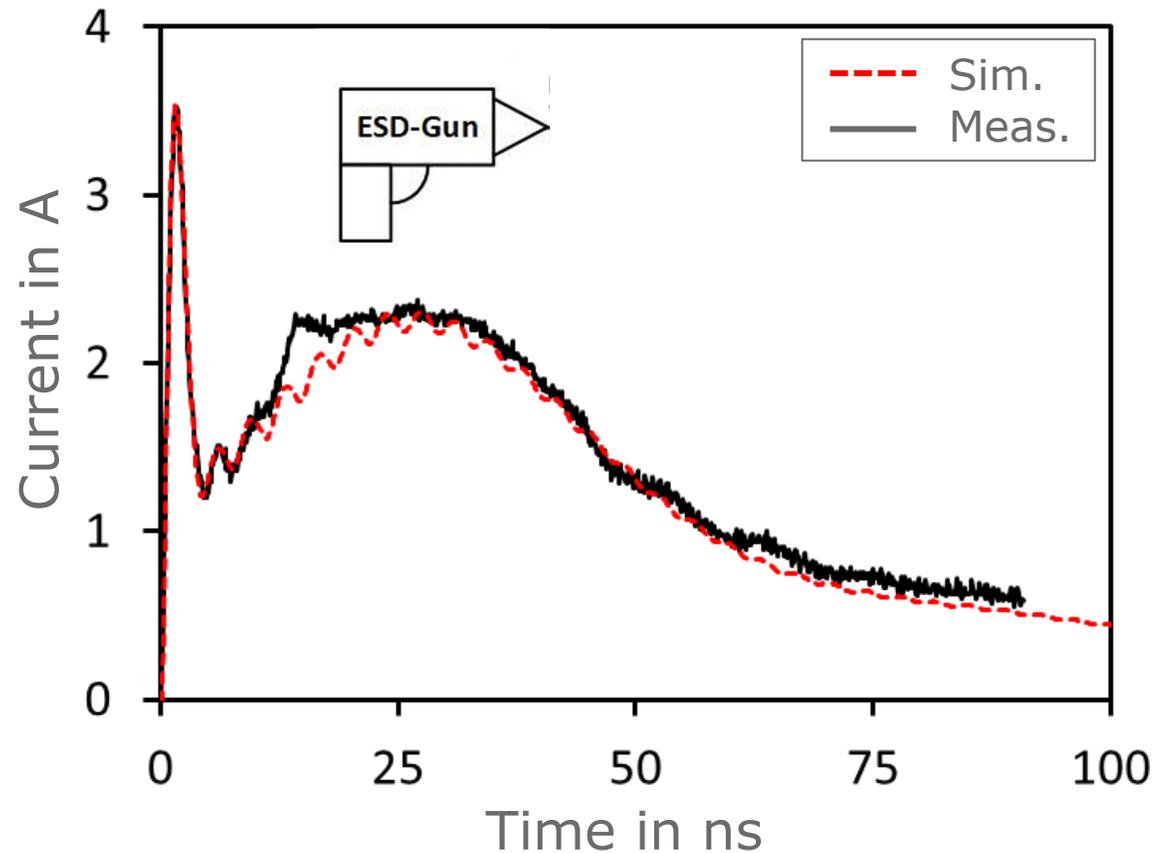
IEEE 100BASE-T1 EMC Test Specification for ESD suppression devices Version 1.0	
<b>OPEN ALLIANCE</b>	
Author & Company	Dr. Bernd Körber, FTZ Zwickau
Title	100BASE-T1 EMC Test Specification for ESD suppression devices
Version	1.0
Date	October 29, 2017
Status	Final
Restriction Level	Public
This measurement specification shall be used as a standardized common scale for EMC evaluation of ESD suppression devices for 100BASE-T1 in automotive applications.	

# Model Types Applied to Realise the SEED Model



# Modelling of ESD Generator

1 kV discharge in 2 Ohm Pellegrini Target (acc. IEC 61000-4-2)

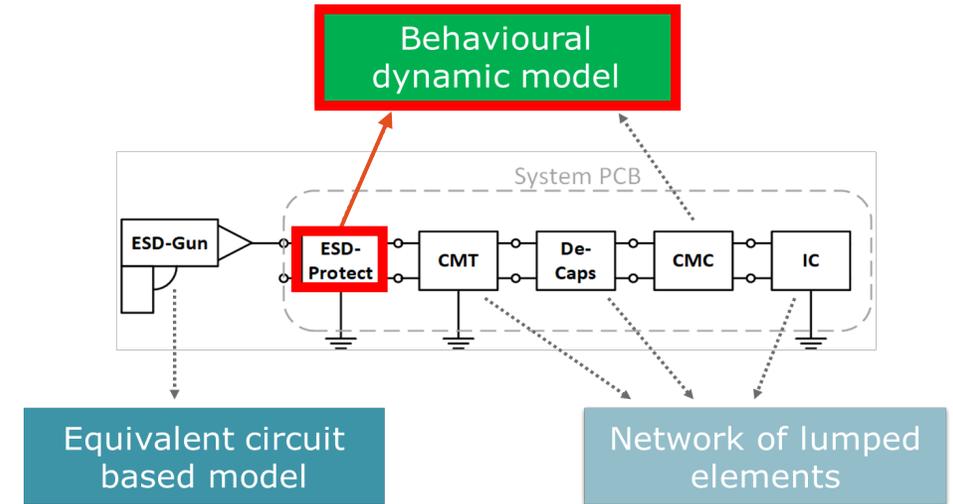
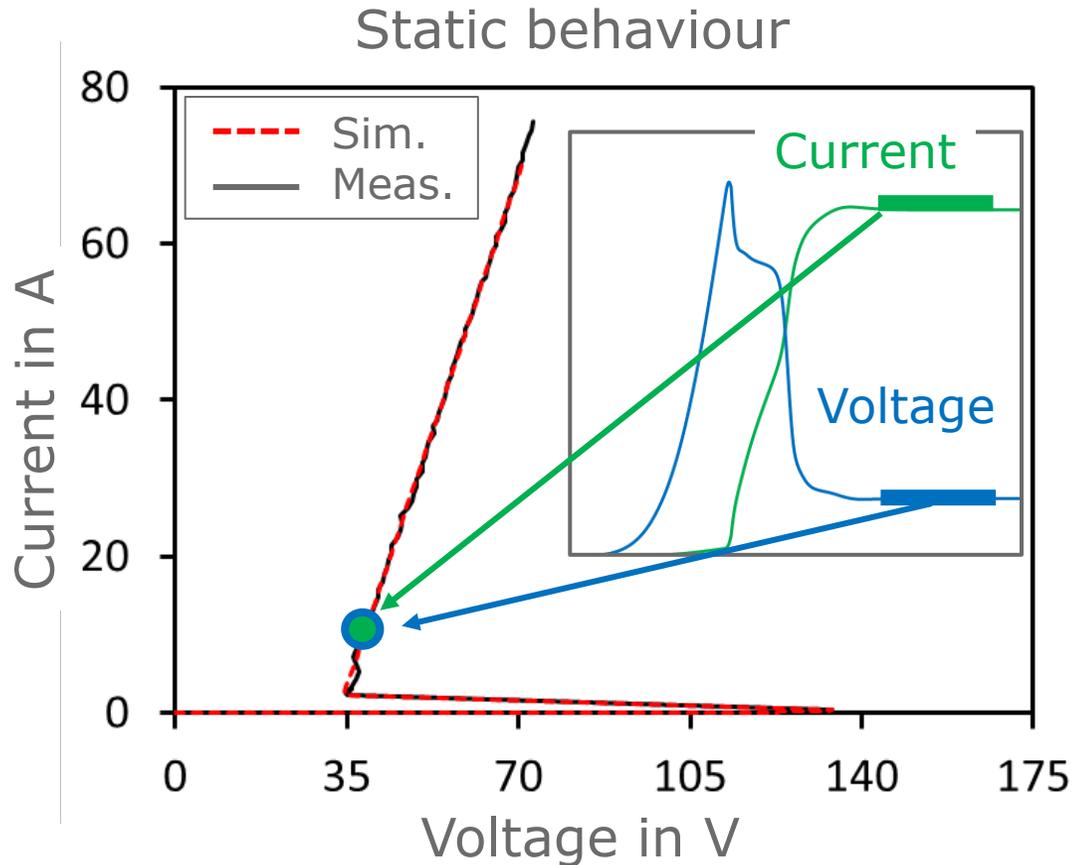


- Entire shape of ESD generator model is **replicated with very high precision** and corresponds to IEC61000-4-2

The extended ESD generator model used here, is based on paper: S.Yang et al., "Effect of Different Load Impedances on ESD Generators and SPICE Models", IEEE 2017

# Modelling of ESD Protection Device

Fully dynamic model of the ESD Protection Device

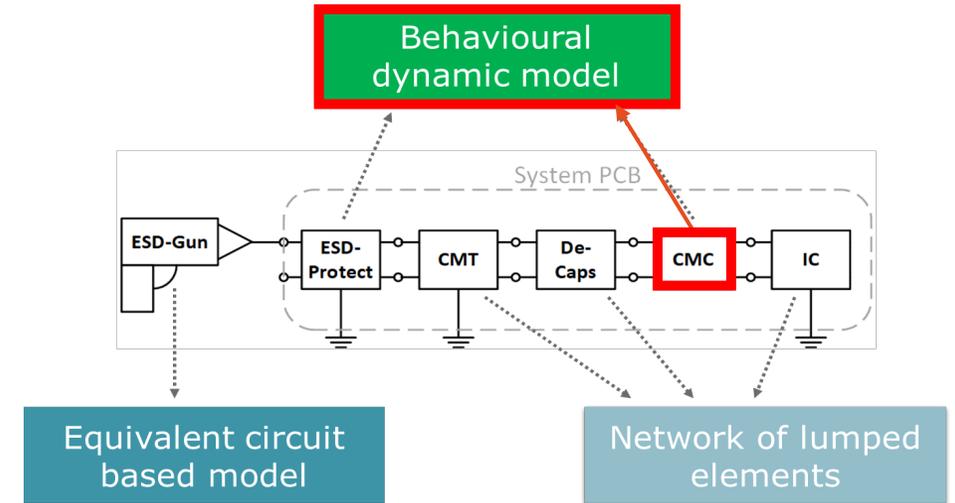
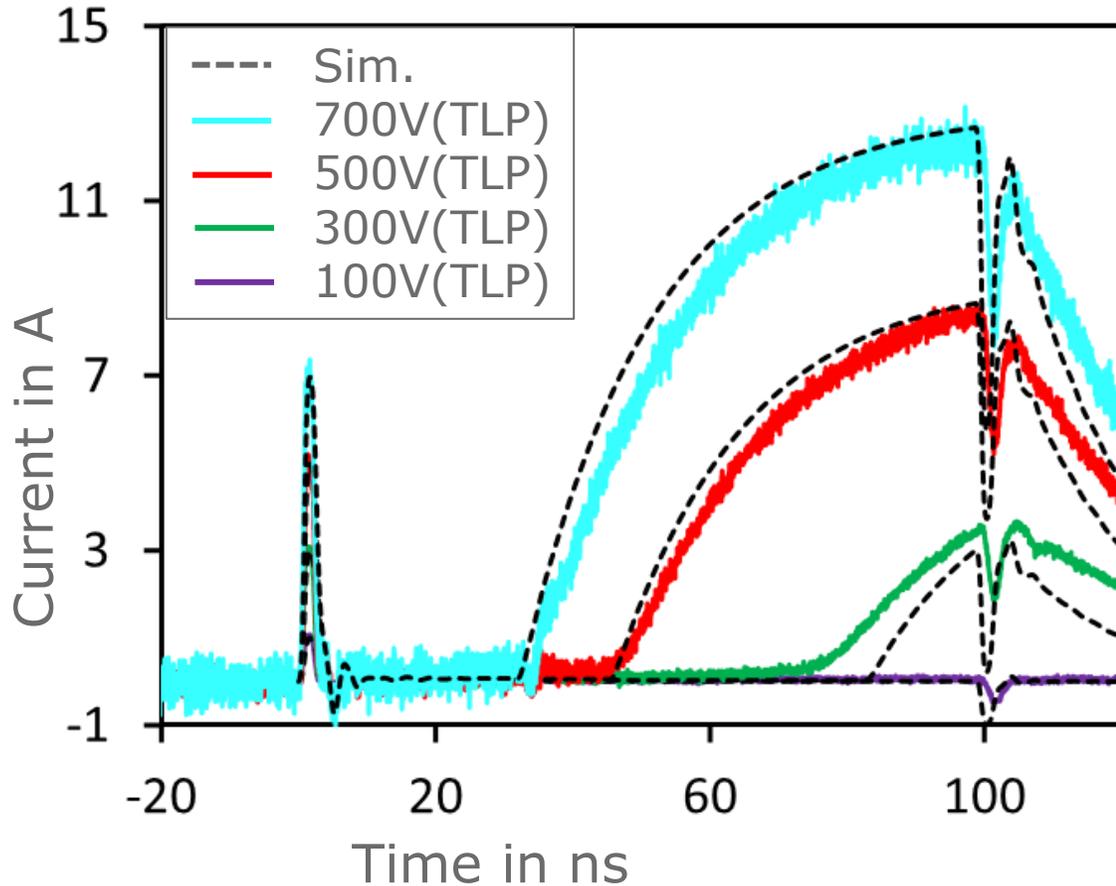


- The ESD Protection is modeled using TLP. Not only the static behavior is modeled but also the dynamic behavior using peak voltages of each TLP pulse

The extended dynamic model used here, is based on paper: P.Weil et al., "TVS Transient Behavior Characterization and SPICE-Based Behavior Model", 40<sup>th</sup> EOS/ESD Symposium, 2018

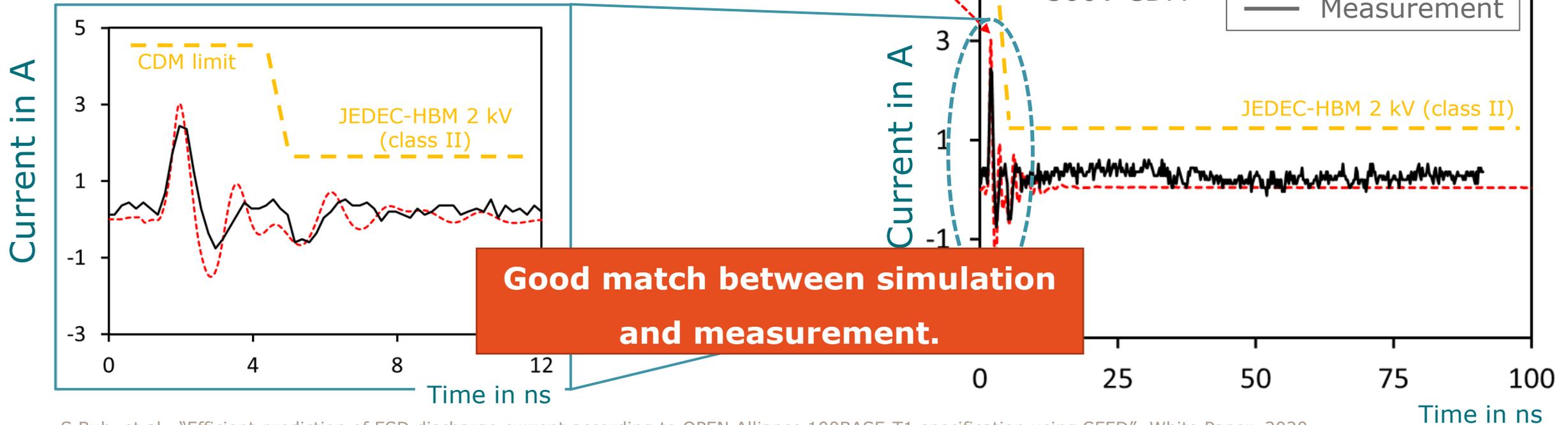
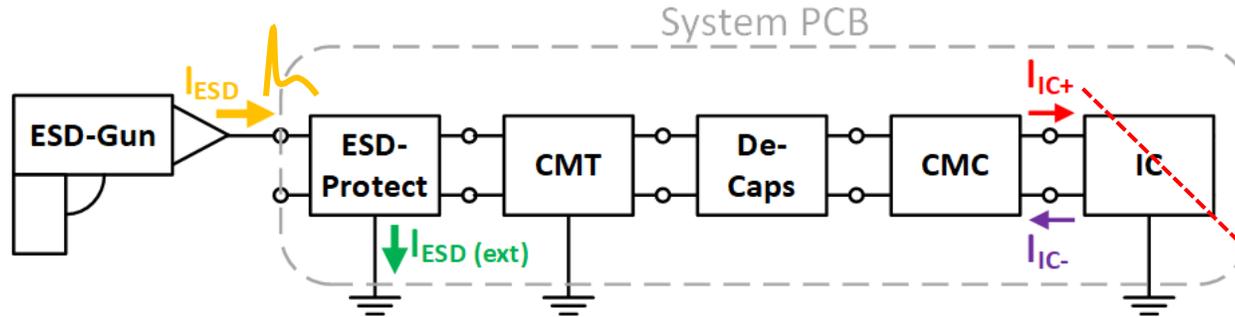
# Modelling of CMC

Simulation fits well the measurements



- The CMC Protection is modeled using TLP measurement similar to the modeling of the ESD device.

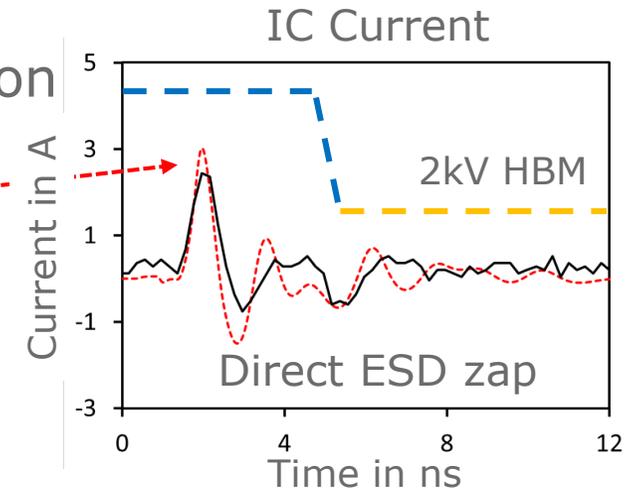
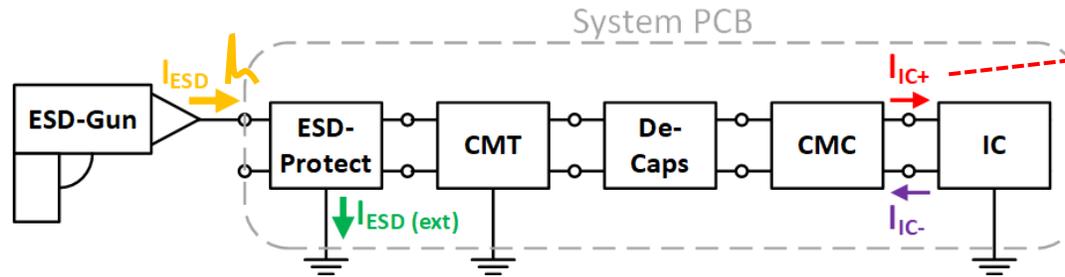
# IC Current after ESD Generator Pulse of 4kV



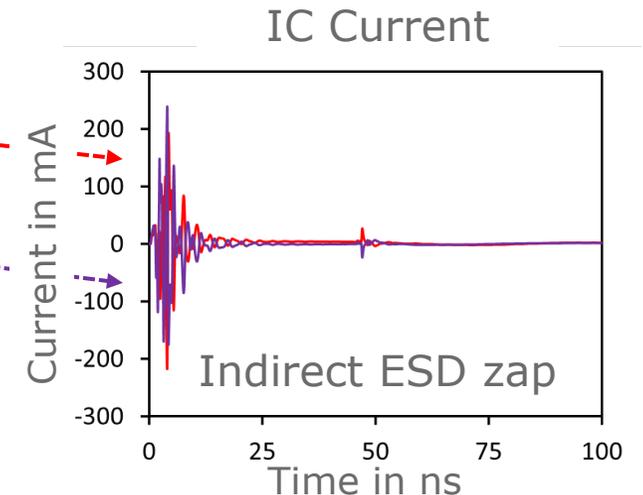
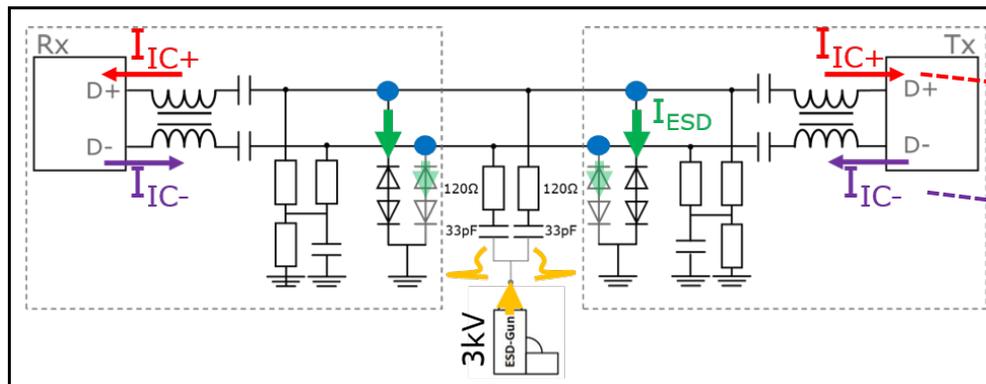
S.Sub, et al., "Efficient prediction of ESD discharge current according to OPEN Alliance 100BASE-T1 specification using SEED", White Paper, 2020

# Summary SEED Simulation

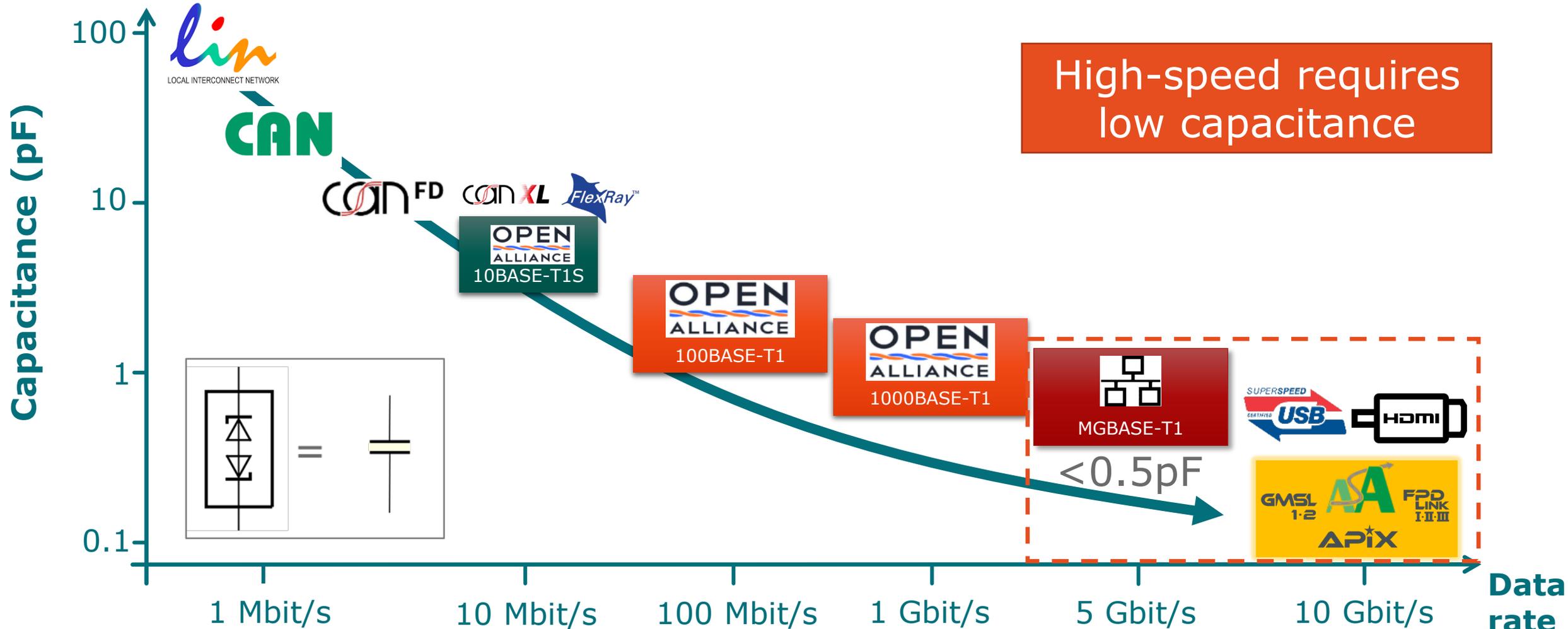
- SEED predicts rest currents into the IC for direct ESD injection



- System Model can be also extended for transient analysis of coupled ESD injections

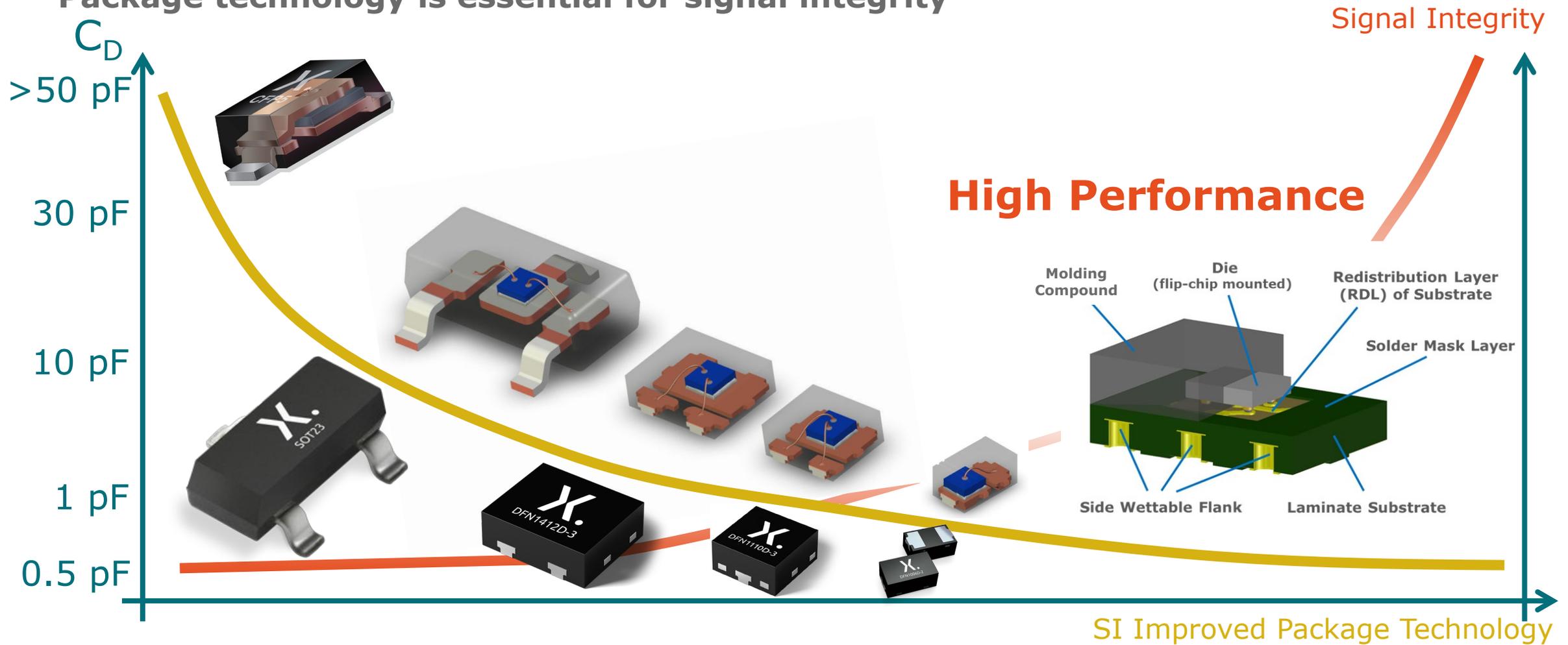


# Application overview: capacitance vs. data rate



# High performance package approaches: FCLGA

Package technology is essential for signal integrity



# Multigigabit Ethernet: Possible ESD Circuitry

	1. Differential HV ESD + CMC	2. Differential LV ESD w CMC	3. Differential LV ESD wo CMC
SCH			
Electrical Performance			
CMC	~ $\mu$ H Range	~nH Range	--
Benefits	<ul style="list-style-type: none"> <li>• ESD Performance</li> <li>• All circuitry is protected</li> <li>• HV Boardnet 48V</li> <li>• PoDL - ready</li> <li>• EM immunity</li> </ul>	<ul style="list-style-type: none"> <li>• Best clamping</li> <li>• ESD and EMI</li> </ul>	<ul style="list-style-type: none"> <li>• Low cost</li> <li>• SI Performance</li> </ul>

Plus further application & quality requirements e.g. 2x AEC-Q101 /  $T_j = 175\text{ }^\circ\text{C}$

# Conclusion & Outlook

More on [nexperia.com](http://nexperia.com)



## New requirements – new solutions

### Automotive Trends



Electrification



Connectivity



Autonomous Driving

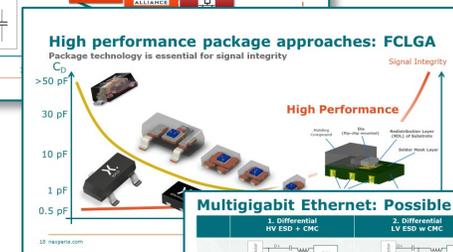
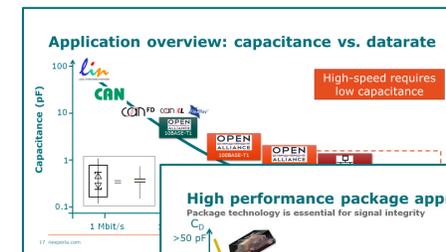
### Efficiency through Simulations

#### Summary SEED Simulation

- SEED predicts rest currents into the IC for direct ESD injection

16 nexperia.com

IEEE SA STANDARDS ASSOCIATION



#### Multigigabit Ethernet: Possible ESD Circuitry

	1. Differential HV ESD + CMC	2. Differential LV ESD w CMC	3. Differential LV ESD w/ CMC
SCM			
Electrical Performance			
CMC	-µF Range	-µF Range	-nF Range
Benefits	-ESD Performance -All circuitry is protected -HV Boardnet 48V -Pb-free ready -EM immunity	-Best damping -ESD and EMI	-Low cost -SI Performance

Plus further application & quality requirements e.g. 2x AEC-Q101 / T<sub>1</sub> = 175 °C

IEEE SA STANDARDS ASSOCIATION



EFFICIENCY WINS.